Amendment to the Abstract:

The Abstract has been amended. A revised Abstract is attached.

Attachment

A bandpass delta sigma truncator ~~comprising input means for receiving~~receives a series of first multi-bit digital signals each having a number of data bits, a first number of sign bits and sign extending means for sign extending each of the first multi-bit digital signals to a second multi-bit digital signal having the same number of data bits as the number of data bits in the first multi-bit digital signals, and a second number of sign bits. ~~output means for supplying from~~ The tractor outputs from a series of third multi-bit digital signals ~~each individually associated with one of the second multi-bit digital signals and each having the same number of data bits as in an associated second multi-bit digital signal. A~~a series of fourth multi-bit digital signals each having a selected number of the most significant data bits of the third multi-bit digital signals, and a series of fifth multi-bit digital signals each having the remaining number of the least significant data bits of the third multi-bit digital signals. ~~means for delaying by a period of time equal to the time between successive first multi-bit digital signals each of the fifth multi-bit digital signals and delaying by a period of time equal to twice the time between successive first multi-bit digital signals each of the fifth multi-bit digital signals and inverting the fifth multi-bit digital signals that have been delayed by a period of time equal to twice the time between successive first multi-bit digital signals means for multiplying by a multiplier number related to the ratio of a selected frequency to the frequency of the first multi-bit digital signals each of the fifth multi-bit digital signals delayed by a period of time equal to the time between successive first multi-bit digital signals and developing a series of sixth multi-bit digital signals having a number of data bits that is the product of the multiplier number and the number of data bits in the fifth multi-bit digital signals and summing means for adding to each second multi-bit digital signal a fifth multi-bit digital signal that has been delayed by a period of time equal to twice the time between successive first multi-bit digital signals and inverted, and a sixth multi-bit digital signal to develop the series of third multi-bit digital signals.~~